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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/466,180	12/17/1999	DONALD F. CAMERON	219.373373X0	9860

23838 7590 08/26/2005

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/466,180	CAMERON ET AL.	
	Examiner	Art Unit	
	Denise Tran	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-12 and 14-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-12 and 14-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The applicant's amendment filed 6/2/05 has been considered. Claims 1, 3-4, 6-12, and 14-30 are presented for examination. Claims 2, 5, and 13 have been canceled.

2. The applicant is nonresponsive to this matter, claiming for priority. **Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120** as follows:

3. This application is claiming the benefit of a prior filed nonprovisional application under 35 U.S.C. 120, 121, or 365(c). Copendency between the current application and the prior application is required.

4. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The specific reference to any prior nonprovisional application must include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

5. If applicant desires priority under 35 U.S.C. 119 (e) based upon the provisional application 60/135,259, Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 119 (e) as follows:

6. The later-filed application must be an application for a patent for an invention which is also disclosed in the prior application (the parent or original nonprovisional application or provisional application); the disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the requirements of the first paragraph of 35 U.S.C. 112. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994).

7. Applicant's claim for domestic priority under 35 U.S.C. 119(e) based upon the provisional application 60/135,259 is acknowledged. However, the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 1, 3-4, 6-12, and 14-30 of this application. In particular, the provisional application 60/135,259 fails to provide adequate support for "a mechanism to flush individual TPT entries stored in the storage device in accordance with a corresponding translation cacheable flag included in the individual TPT entry" claim 6, lines 6-7. Claims 1, 9, 21, and 26 have similar problems as discussed above.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3-4, 6-12, and 14-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (5,937,436), in view of Horstmann et al., U.S. Patent No. 6,125,433, (hereinafter Horstmann), further in view of Futral et al., U.S. Patent No. 5,991,797 (hereinafter Futral 797), and further in view of Garcia et al., U. S. Patent No. 6,163,834 (hereinafter Garcia). The rejections are maintained.

As per claim 1, Watkins shows of the invention substantially as claimed, a work station (e.g., fig.2A, el. 200, col. 3, line 34) coupled to a switched fabric (e.g., fig.3, an ATM Switch and network; col. 3, lines 14-18), comprising:

a processor (e.g. figure 2A, element 210);

a main memory coupled to the processor (e.g. figure 2A, element 220); and

a workstation fabric adapter (e.g. figure 2A, element 260K) coupled to the processor and provided to interface with the switched fabric (e.g., fig.3, an ATM Switch and network; col. 3, lines 14-18), which caches (i.e., frequently used data values being duplicated for quick access) selected translation and protection table (TPT) entries from the memory for a data transaction (e.g., figure 4, element 450 and col. 2, lines 14-18; col. 1, lines 54-65; col. 6, lines 5-14; col. 6, lines 49-65 and col. 7, lines 60-65), each TPT entry comprising protection attributes to control read and write access to a given memory region of said memory (e.g., col. 4, lines 35-50), a physical page address field to address a physical page frame of data entry (e.g., col. 4, lines 35-50) and flushes

individual cached TPT entries from said internal cache(e.g. col. 2, lines 19-22, col. and col. 9, lines 13-15 and 65).

Watkins does not explicitly show the use of flushing in accordance with a translation cacheable flag to specify whether said adapter may flush a corresponding TPT entry. Horstmann shows the use of flushing individual table entry in accordance with a corresponding translation cacheable flag to specify whether a table may flush a corresponding TPT entry (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed by limiting number of reloading currently used data, reduce chip area for fabrication, support efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses.

Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

Watkins, Horstmann, and Futral 797 do not explicitly show a memory protection tag to specify whether said adapter has permission to access said memory. Garcia shows a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2, lines 20-55). It would have been obvious to one ordinary skill in the art at the time the invention was made to apply the teaching of Garcia into the combine system of Watkins, Horstmann and Futral 797 because it would allow a network adapter to perform protection checking and invalid access.

As per claim 3, Watkins shows the use of each of the selected translation and protection table entries as a page of the main memory (e.g. col. 3, lines 28-33 and col. 6, lines 55-60). Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

As per claim 4, Watkins shows the use of the adapter is provided to perform virtual to physical address translations and validate access to the memory using the selected translation and protection table entries (e.g. col. 2, lines 14-22 and col. 6, lines 43-65 and figure 5, col. 7, line 5, lines 59-63 and col.1, lines 64-68). Watkins and

Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

As per claims 6, 14, 20, 25 and 30, Watkins shows said protection attributes comprise a memory write enabled flag to indicate whether said adapter can write to a page (e.g., col. 4, lines 35-50). Watkins, Horstmann, and Futral 797 do not explicitly show a RDMA read enable flag to indicate whether the page can be a source of a RDMA read operation and a RDMA write enable flag to indicate whether the page can be a target of a RDMA write operation. Garcia shows a RDMA read enable flag to indicate whether the page can be a source of a RDMA read operation and a RDMA write enable flag to indicate whether the page can be a target of a RDMA write operation (e.g., fig. 6, RDMARead and RDMAWrt, col. 2, lines 20-55). It would have been obvious to one ordinary skill in the art at the time the invention was made to apply the teaching of Garcia into the combine system of Watkins, Horstmann and Futral because it would allow an network adapter to perform protection checking and invalid access.

As per claim 7, the combination of Watkins, Horstmann , Futral 797, and Garcia teach the claimed invention as discussed above. Also, Watkins does not explicitly shows said host adapter flushes a designated cached TPT entry from said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a first logic state, and maintains said designated cached translation cacheable flag of said designated cached TPT entry in said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a second logic state opposite of said first logic state. Horstmann shows flushes a designated cached TPT entry from an internal cache when a translation cacheable flag of said designated cached TPT entry indicates a first logic state, and maintains said designated cached translation cacheable flag of said designated cached TPT entry in said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a second logic state opposite of said first logic state (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed by limiting number of reloading currently used data, reduce chip area for fabrication, support efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses.

As per claim 8, Watkins shows the use of the adapter flushing of a table entry by software (e.g., col.7, lines 26-27 and col.10, lines 26-28). Watkins does not specifically show the use of an operating system including driver software to set the status of the

translation cacheable flag per translation and protection table entry for enabling flushing individual cached translation and protection table entry from the internal cache. Horstmann shows an operating system (e.g., col. 1, lines 16-19); and software of the operating system setting the status of the translation cacheable flag per translation and protection table entry for enabling flushing individual cached translation and protection table entry from the internal cache (e.g., col. 11, lines 25-35 and col. 10, lines 1-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of the operating system of Horstmann into the system of Watkins because it would provide efficiently supporting overall control of many concurrent processes running within the system, supervising the allocation and usage of system hardware resources such as setting the status of the translation cacheable flag per translation and protection table entry for enabling flushing individual cached translation and protection table entry from the internal cache as taught by Horstmann, col.1, lines 41-55 and col. 11, lines 25-35; thereby it would increase translation speed by limiting number of reloading currently used data, reduce chip area for fabrication, supports efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses.

Watkins, Horstmann, and Futral 797do not specifically show the use of a driver to run an adapter. Garcia show the use of driver (e.g., col. 1, lines 50-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a driver for the adapter to the combined system of Watkins, Horstmann, and

Futral 797 because it would allow the operating system to communicate with the internal components to update, complete transactions with and control a variety of I/O interfaces, such as network interface.

As per claim 9, Watkins shows a network (e.g., ATM network col. 3, lines 10-20), comprising:

a switched fabric (e.g. figure 3, an ATM switch and network and col. 3, lines 10-20); and

a workstation (e.g. figure 2A, element 200) comprising a main memory (e.g. figure 2A, element 220), a workstation fabric adapter (e.g. figure 2A, element 260k) which caches (i.e., frequently used data values being duplicated for quick access) selected translation and protection table (TPT) entries from the main memory (e.g., figure 4, element 450 and col.1, lines 54-65; col. 2, lines 14-22; col. 6, lines 5-10; col. 6, lines 49-65 and col. 7, lines 60-65), each TPT entry comprising protection attributes to control read and write access to a given memory region of said memory (e.g., col. 4, lines 35-50), a physical page address field to address a physical page frame of data entry (e.g., col. 4, lines 35-50) and flushes individual cached TPT entries from said internal cache(e.g. col. 2, lines 19-22, col. and col. 9, lines 13-15 and 65).

Watkins does not explicitly show the use of flushing in accordance with a translation cacheable flag and an operating system. Horstmann shows the use of flushing individual table entry in accordance with a corresponding translation cacheable flag (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35) and the use of operating

system (e.g., col. 1, lines 17-19 and col. 1, lines 49-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching the corresponding translation cacheable flag of Horstmann into the system of Watkins because it would increase translation speed from limiting number of reloading currently used data, reduce chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49. Also, It would have been obvious to one of ordinary skill in the art at the time the invention was made to have apply the teaching operating system of Horstmann into the system of Watkins because it would provide the overall control of many concurrent processes running within the system, supervising the allocation and usage of system hardware resources, scheduling operations and preventing interference between different programs as teaching in Horstmann col.1, lines 39-55.

Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

Watkins, Horstmann, and Futral 797 do not explicitly show a memory protection tag to specify whether said adapter has permission to access said memory. Garcia

shows a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2, lines 20-55). It would have been obvious to one ordinary skill in the art at the time the invention was made to apply the teaching of Garcia into the combine system of Watkins, Horstmann and Futral 797 because it would allow an network adapter to perform protection checking and invalid access.

As per claims 10 and 17, Watkins shows the use of the adapter comprises an internal cache memory (i.e., a memory in which frequently used data values being duplicated for quick access) for storing a set of translation and protection table entries from the memory (e.g., figure 4, element 450 and col. 2, lines 14-22; col. 1, lines 54-68; col. 6, lines 3-14; col. 6, lines 49-65 and col. 7, lines 60-65). Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

As per claim 11, Watkins shows the use of each of the selected translation and protection table entries as a page of the main memory (e.g. col. 3, lines 28-33 and col. 6, lines 55-60). Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-

attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

As per claim 12, Watkins shows the use of the adapter is provided to perform virtual to physical address translations and validate access to the memory using the selected translation and protection table entries (e.g. col. 2, lines 14-22 and col. 6, lines 43-65 and figure 5, col. 7, line 5, lines 59-63 and col.1, lines 64-68). Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

As per claim 15, Watkins shows wherein the adapter flushing a cached translation and protection table entry from the internal cache (e.g. col. 2, lines 19-22, col. 6, lines 9-13 and col. 9, lines 9-65). Watkins does not explicitly show flushing a designate cache when the translation cacheable flag of the designated cache table entry indicated a first logic state and maintained the designated table entry for future re-

used when the flag of the designated table entry indicated a second logic opposite of the first logic state. Horstmann shows the use of flushing a designate cache when the translation cacheable flag (e.g., valid bit) of the designated cache table entry indicated a first logic state and maintain the designated table entry for future re-used when the flag of the designated table entry indicated a second logic opposite of the first logic state (e.g. col. 4, lines 30-34, col. 11, lines 25-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed from limiting a number of reloading currently used data, reduced chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses. Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

As per claims 26 and 21, Watkins shows the use of the adapter (e.g., fig. 2A, element 260K) in a system provided to interface a switched fabric (e.g., fig. 3, an ATM Switch and network; col. 3, lines 14-18), comprising: a cache memory (i.e., a memory in

which frequently used data values being duplicated for quick access) for storing a set of translation and protection table entries from the memory (e.g., figure 4, element 450 and col. 2, lines 14-22; col. 1, lines 54-68; col. 6, lines 3-14; col. 6, lines 49-65 and col. 7, lines 60-65) for virtual to physical address translations and access validation to the memory during I/O (e.g. col. 2, lines 14-22 and col. 6, lines 43-65 and figure 5, col. 7, line 5, lines 59-63 and col.1, lines 64-68), each of the TPT entries corresponds to a memory portion of the memory (e.g. col. 2, lines 14-22 and col.1, lines 64-68; col. 3, lines 28-33 and col. 6, lines 55-60) and comprises at least a translation cacheable flag (e.g., col. 6, lines 5-45; col. 8, lines 24-45); and a mechanism to determine a status of the translation cacheable flag of one or more selected TPT entries stored in the cache of the adapter (e.g., col. 6, lines 5-45; col. 8, lines 24-45). Watkins does not explicitly show discarding the one or more selected TPT entries from the cache based on the status of the translation cacheable flag or checking a status of the translation cacheable flag to determine whether to discard one or more selected TPT entries from the cache of the adapter and each TPT entries comprising a memory protection tag to specify whether the adapter has permission to access the host memory. Horstmann shows the use of discarding the one or more selected table entries from the cache based on the status of the translation cacheable flag or using a status of the translation cacheable flag to determine whether to discard one or more selected table entries from the cache of the adapter (e.g., col. 11, lines 25-35; col. 10, lines 1-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed from

limiting a number of reloading currently used data, reduced chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49. Watkins and Horstmann do not explicitly show the use of the workstation being a host. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secured as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

. Watkins, Horstmann, and Futral do not explicitly show a memory protection tag to specify whether said adapter has permission to access said memory. Garcia shows a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2, lines 20-55). It would have been obvious to one ordinary skill in the art at the time the invention was made to apply the teaching of Garcia into the combine system of Watkins, Horstmann and Futral 797 because it would allow an network adapter to perform protection checking and invalid access.

As per claim 16, Watkins shows the invention substantially as claimed, an apparatus, comprising: a storage device to store translation table and protection table (TPT) entries for virtual to physical address translations (e.g., fig. 5; col. 4, lines 35-50, col. 7, lines 55-64), wherein each of said TPT include protection attributes to control read and write access to a given memory region of said memory (e.g., col. 4, lines 35-

50), a physical page address field to address a physical page frame of data entry (e.g., col. 4, lines 35-50; col. 3, lines 20-30) and a mechanism to flush individual TPT entries stored in the storage device (e.g. col. 2, lines 19-22, col. and col. 9, lines 13-15 and 65).

Watkins does not explicitly show the use of flushing in accordance with a translation cacheable flag included in the individual TPT entry. Horstmann shows the use of flushing individual table entry in accordance with a corresponding translation cacheable flag included in the individual TPT entry (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35) (e.g., fig. 6, VB=0; col. 7, lines 6-8; col. 11, lines 34-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed by limiting number of reloading currently used data, reduce chip area for fabrication, support efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses.

Watkins and Horstmann do not explicitly show the use of a host memory. Futral 797shows a host comprising a host memory (e.g. col. 1, lines 52-60; col. 8, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer having a memory storing its data in a system connected by a communication link; and provide data transferring to be controlled and secured as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

Watkins, Horstmann, and Futral 797 do not explicitly show a memory protection tag to specify whether said adapter has permission to access said memory. Garcia shows a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2, lines 20-55). It would have been obvious to one ordinary skill in the art at the time the invention was made to apply the teaching of Garcia into the combine system of Watkins, Horstmann and Futral 797 because it would allow an network adapter to perform protection checking and invalid access.

As per claims 22 and 27, Watkins teaches the use of the adapter and TPT entry as discussed above. Watkins does not explicitly show the use an operating system to set the status of the translation cacheable flag per TPT entry for enabling to discard individual TPT entries from the cache. Horstmann shows the use of an operating system to set the status of the translation cacheable flag per table entry for enabling to discard individual table entries from the cache (e.g. col. 11, lines 25; col. 1, lines 17-19 and col. 1, lines 49-55; col. 10, lines 1-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann into the system of Watkins because it would increase translation speed from limiting number of reloading currently used data, reduce chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49.

As per claims 18, 23, and 28, Watkins shows the use of each of the selected translation and protection table entries represents translation of a single page of the main memory (e.g. col. 3, lines 28-33 and col. 6, lines 55-60). Watkins and Horstmann

do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

As per claims 19, 24, and 29, Watkins, Horstmann, Futral 797, and Garcia show the claimed invention as discussed above. Also, Watkins shows each TPT entry comprising protection attributes to control read and write access to a given memory region of said memory (e.g., col. 4, lines 35-50), a physical page address field to address a physical page frame of data entry (e.g., col. 4, lines 35-50; col. 3, lines 20-30) and flushes individual cached TPT entries from said internal cache(e.g. col. 2, lines 19-22, col. and col. 9, lines 13-15 and 65).

Watkins does not explicitly show the use of flushing in accordance with a translation cacheable flag to specify whether said adapter may flush a corresponding TPT entry. Horstmann shows the use of flushing individual table entry in accordance with a corresponding translation cacheable flag to specify whether a table may flush a corresponding TPT entry (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed by limiting number of reloading currently used data, reduce chip area

for fabrication, support efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses.

10. Applicant's arguments filed 6/2/05 have been fully considered but they are not persuasive.

11. In the remarks, the applicant argued that the cited reference do not teach "a host couple to a switched fabric including one or more . . . each TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory, . . . protection attributes to control read and write access to a given memory region of a host memory . . . and a memory protection tag to specify whether said apparatus has permission to access said host memory . . . "

The examiner disagreed with the applicant's arguments because the combination of Watkins, Horstman, Futral 797, and Garcia teaches the claimed invention. In particular, Watkins shows a work station (e.g., fig.2A, el. 200, col. 3, line 34) coupled to a switched fabric (e.g., fig.3, an ATM Switch and network; col. 3, lines 14-18), comprising:

a processor (e.g. figure 2A, element 210);

a main memory coupled to the processor (e.g. figure 2A, element 220); and

a workstation fabric adapter (e.g. figure 2A, element 260K) coupled to the processor and provided to interface with the switched fabric (e.g., fig.3, an ATM Switch

and network; col. 3, lines 14-18), which caches (i.e., frequently used data values being duplicated for quick access) selected translation and protection table (TPT) entries from the memory for a data transaction (e.g., figure 4, element 450 and col. 2, lines 14-18; col. 1, lines 54-65; col. 6, lines 5-14; col. 6, lines 49-65 and col. 7, lines 60-65), each TPT entry comprising protection attributes to control read and write access to a given memory region of said memory (e.g., col. 4, lines 35-50), a physical page address field to address a physical page frame of data entry (e.g., col. 4, lines 35-50) and flushes individual cached TPT entries from said internal cache(e.g. col. 2, lines 19-22, col. and col. 9, lines 13-15 and 65).

Watkins does not explicitly show the use of flushing in accordance with a translation cacheable flag to specify whether said adapter may flush a corresponding TPT entry. Horstmann shows the use of flushing individual table entry in accordance with a corresponding translation cacheable flag to specify whether a table may flush a corresponding TPT entry (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed by limiting number of reloading currently used data, reduce chip area for fabrication, support efficient operation as taught by Horstmann, col. 4, lines 43-49; and provide for efficient operation of the translation entries by making sure there is room in the translation table for new addresses.

Watkins and Horstmann do not explicitly show the use of the workstation being a host and having one or more fabric-attached I/O controllers. Futral 797 shows the use

of a host (e.g. figure 2, el. 20) and fabric-attached I/O controllers (e.g. fig. 2, el. 32, 52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and allow data transferring to be controlled and secure as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60.

Watkins, Horstmann, and Futral 797 do not explicitly show a memory protection tag to specify whether said adapter has permission to access said memory. Garcia shows a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2, lines 20-55). It would have been obvious to one ordinary skill in the art at the time the invention was made to apply the teaching of Garcia into the combine system of Watkins, Horstmann and Futral 797 because it would allow a network adapter to perform protection checking and invalid access.

12. In the remarks, the applicant argued that Watkins do not teach " . . . protection attributes to control read and write access to a given memory region of a host memory . . ." as disclosed in the embodiments of claim 1 and the protection bits disclosed in Watkins are directed toward the ATU not toward a memory unit

The examiner disagreed with the applicant's arguments because Watkins shows wherein each of said TPT include protection attributes to control read and write access to a given memory region of said memory (e.g., col. 4, lines 35-50). According to

Watkins, fig. 5, col. 4, lines 35-45 teaches the protection bits transferred through control lines 560 of fig. 5 in determining whether a page is accessible using the ATU's physical translation for the virtual address (wherein a physical address toward a memory unit, col. 1, lines 55-56) and a read only page can be protected from writes with a read only page protection bit. Also, fig. 5 and col. 7, lines 55 and 60-65, Watkins teaches the physical address (i.e., memory region; physical address toward a memory unit, col. 1, lines 55-56) outputting under all condition unless the protection bits 560 signify that the cycle in progress is prohibited due to an attempted write access of a read-only page. Therefore, the protection bits disclosed in Watkins are directed toward the ATU not toward a memory unit.

In addition, Watkins and Horstmann do not explicitly show the use of a host memory. Futral 797shows a host comprising a host memory (e.g. col. 1, lines 52-60; col. 8, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer having a memory storing its data in a system connected by a communication link; and provide data transferring to be controlled and secured as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60. Thus, the cited references teaches " . . . protection attributes to control read and write access to a given memory region of a host memory. . ." as disclosed in the embodiments of claim 1.

13. In the remarks, the applicant's argued that nowhere in the Garcia reference disclosed a memory protection tag to specify whether said host fabric adapter has permission to access a host memory.

The examiner disagreed with the applicant's argument because Garcia teaches a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2, lines 20-55). In particular, Garcia teaches a network interface controller NIC (adapter) copies data from memory to a network medium and from the medium to the memory (e.g., col. 1, lines 45-55) and only memory that has been registered with the NIC and Kernel Agent can be used for data transfers (e.g., col. 2, lines 1-2). According to fig. 6 and col. 2, lines 40-55, Garcia teaches the NIC has access to the memory protection tags and compares the values to detect invalid accesses of a memory (i.e., a memory tag to specify whether an adapter has permission to access a memory). In addition, Watkins and Horstmann do not explicitly show the use of a host memory. Futral 797 shows a host comprising a host memory (e.g., col. 1, lines 52-60; col. 8, lines 20-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral 797 with Watkins and Horstmann because it would provide a main computer having a memory storing its data in a system connected by a communication link; and provide data transferring to be controlled and secured as taught by Futral 797 col. 1, lines 60-65 and col. 2, lines 55-60. Thus, the cited references teaches disclosed a memory protection tag to specify whether said host fabric adapter has permission to access a host memory.

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and Friday from 8:45 a.m. to 5:15 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

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D.T.
8/22/05